

FIG. 1

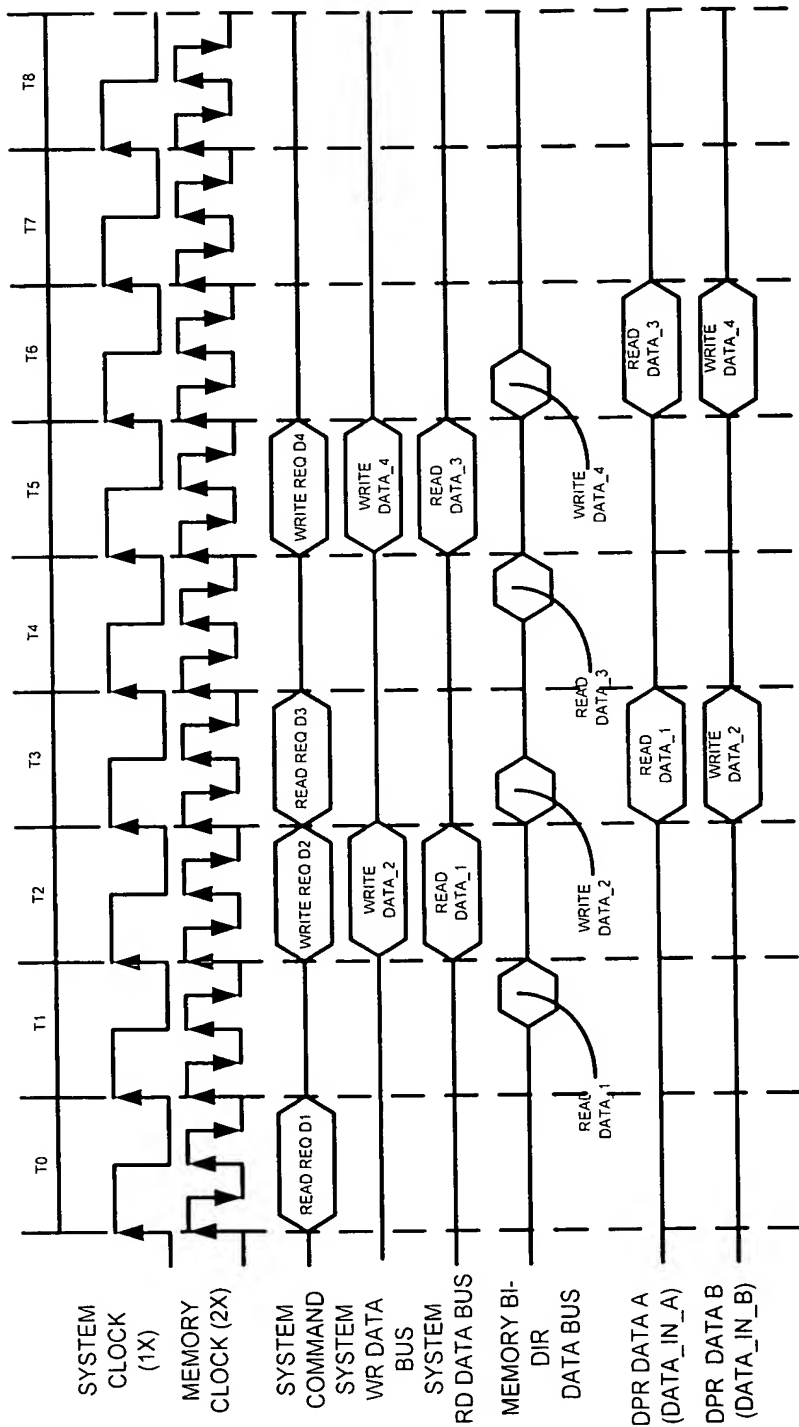


FIG. 2

T0	- CPU REQUESTS READ 1
T1	- READ DATA_1 IS PUSHED ONTO MEMORY BUS BY CPU - CPU PERFORMS WRITE 2
T2	- WRITE DATA_2 IS PUSHED ONTO SYSTEM BUS BY CPU - READ DATA_1 IS PUSHED ONTO SYSTEM BUS BY SYNCHRONIZER
T3	- CPU REQUESTS READ 3 - WRITE DATA_2 IS PUSHED ONTO MEMORY BUS BY SYNCHRONIZER - ADDR+DATA CTL FOR READ CYCLE WRITES DATA TO DPR - ADDR+DATA CTL FOR WRITE CYCLE WRITES DATA TO DPR
T4	- READ DATA_3 IS PUSHED ONTO MEMORY BUS BY CPU - CPU REQUESTS WRITE 4
T5	- WRITE DATA_4 IS PUSHED ONTO SYSTEM BUS BY CPU - READ DATA_3 IS PUSHED ONTO SYSTEM BUS BY SYNCHRONIZER
T6	- WRITE DATA_4 IS PUSHED ONTO MEMORY BUS BY THE SYNCHRONIZER - ADDR+DATA CTL FOR READ CYCLE WRITES DATA TO DPR - ADDR+DATA CTL FOR WRITE CYCLE WRITES DATA TO DPR

FIG. 3

DUAL PORT RAM
(DPR)

ADDRESS LOCATION	DATA
A_x	READ DATA_1
A_{x+1}	WRITE DATA_2
A_{x+2}	READ DATA_3
A_{x+3}	WRITE DATA_4